

CHE323/CHE384  
 Chemical Processes for Micro- and Nanofabrication  
[www.lithoguru.com/scientist/CHE323](http://www.lithoguru.com/scientist/CHE323)

## Lecture 27 Device Isolation

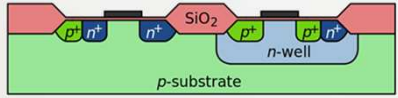
Chris A. Mack  
 Adjunct Associate Professor

**Reading:**  
 Chapter 15, *Fabrication Engineering at the Micro- and Nanoscale*, 4<sup>th</sup> edition, Campbell

© Chris Mack, 2013 1

## Device Isolation

- A silicon wafer will conduct. Two transistors located close to each other on the wafer will be electrically connected via the substrate



- Device isolation is used to prevent separate transistors from interacting with each other through the substrate
  - Goal: good isolation while consuming the smallest area of silicon

© Chris Mack, 2013 2

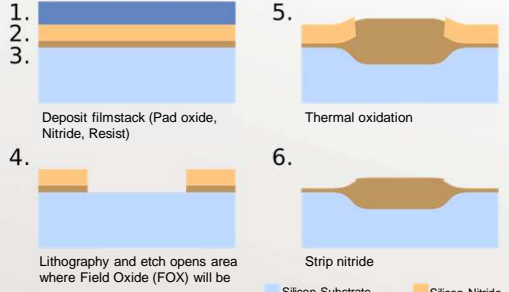
## Device Isolation

- There are two common approaches to device isolation
- LOCOS – Local Oxidation of Silicon
  - Popular in the 1970s and 1980s
- STI – Shallow Trench Isolation
  - Came in to use in the 1990s
  - Preferred method for 250 nm technologies and below

© Chris Mack, 2013 3

## LOCOS Process

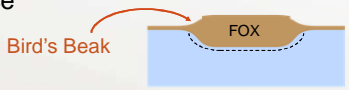
1. Deposit filmstack (Pad oxide, Nitride, Resist)
- 2.
- 3.
4. Lithography and etch opens area where Field Oxide (FOX) will be
5. Thermal oxidation
6. Strip nitride



© Chris Mack, 2013 (Image from Wikimedia Commons) 4

## LOCOS Process

- Bird's beak encroaches on active area, using up space

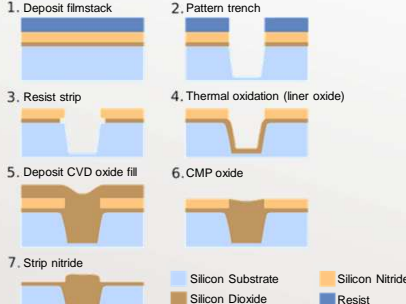


- Better isolation comes from thicker oxide, but this leads to larger bird's beak
- Usually a field implant is carried out just before oxidation (to increase  $V_{th}$  of parasitic MOSFET)

© Chris Mack, 2013 5

## Shallow Trench Isolation Processes

1. Deposit filmstack
2. Pattern trench
3. Resist strip
4. Thermal oxidation (liner oxide)
5. Deposit CVD oxide fill
6. CMP oxide
7. Strip nitride




(Image from Wikimedia Commons)  
 © Chris Mack, 2013 6

THE UNIVERSITY OF TEXAS  
AT AUSTIN

WHAT STARTS HERE CHANGES THE WORLD

## STI Process

- Now the dominant isolation approach
- Uses less area, allowing greater transistor density
- Trench depth can be large (~500nm) even as trench width decreases
- Requires well controlled deep etches, good oxide CVD process, and CMP



© Chris Mack, 2013 7

THE UNIVERSITY OF TEXAS  
AT AUSTIN

WHAT STARTS HERE CHANGES THE WORLD

## Lecture 27: What have we learned?

- Why is device isolation needed?
- What are the two most common device isolation processes?
- Why is STI the more common today?

© Chris Mack, 2013 8