Interconnect Delay

- The speed of a chip is a function of how fast transistors can be switched on and off, and how fast signals can propagate along the wires connecting them
- Dennard scaling
  - Transistor switching time decreased regularly till the early 2000s
  - Interconnect delay time increased during this time, since the length of interconnect wires has remained roughly constant
- Result: Interconnect delay is now equally or more important in determining chip speed as transistor delay

Interconnect Delay

\[ \tau = \text{rise time/fall time} = \text{interconnect delay} = RC \]

- \( R = \text{resistance} = \text{resistivity} \cdot \frac{\text{length}}{\text{cross-section area}} \)
- \( C = \text{capacitance} = \text{dielectric constant} \cdot \frac{\text{plate area}}{\text{gap width}} \)

How Can \( \tau \) Be Reduced?

1. Reduce metal resistivity
   - \( \rho_{\text{Al}} = 2.8 \times 10^{-6} \, \Omega \, \text{cm} \)
   - \( \rho_{\text{Cu}} = 1.7 \times 10^{-6} \, \Omega \, \text{cm} \)
2. Reduce insulator dielectric constant
   - \( \varepsilon_{\text{SiO}_2} = K_{\text{SiO}_2} \varepsilon_0 = 3.9 \)
   - For “low-K” dielectrics, we want \( K_{\text{SiO}_2} \approx 2 - 2.5 \)
   - Use polymers, fluorinated oxides, porous oxides: this is very hard to do!
How Can $\tau$ Be Reduced?

3. Make $t_{\text{m}}, t_{\text{ox}}$ thicker
   - Results in greater topography
   - Limited by metal line aspect ratio

4. Make metal pitch ($= w_{\text{m}} + w_{\text{s}}$) bigger
   - Requires more metal levels

5. Reduce $L$ by using pass transistors
   - Do this when interconnect delay $> 2 \times$ transistor delay

\[ \tau = \rho_{\text{m}} t_{\text{m}} \frac{I^2}{W_{\text{m}}} \] \[ \tau = \rho_{\text{ox}} t_{\text{ox}} \frac{I^2}{W_{\text{m}}} \]

Interconnect Delay

- We’ve switched from aluminum to copper, but from here things get exotic (carbon nanotubes, etc.)
- Low-K dielectrics are hard to make and use
  - Low-K usually results in low mechanical strength
- There is a big cost to making metal lines wider and/or thicker
- Pass transistors use up area, and so are costly

Lecture 29: What have we learned?

- Why is interconnect such a big problem today?
- What gives rise to interconnect delay?
- What are five ways to reduce interconnect delay?