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CHE323/CHE384  
Chemical Processes for Micro- and Nanofabrication

# Lecture 9 CMOS Process Flow

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**Reading:**  
Chapter 16, *Fabrication Engineering at the Micro- and Nanoscale*, 4<sup>th</sup> edition, Campbell

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## Basic CMOS Process Flow

0. Wafer Prep: Laser Scribe, Clean, gettering, 0<sup>th</sup> layer Alignment Marks
1. N-Well and P-Well Diffusion
2. Active Area
3. Polysilicon Gate
4. Lightly Doped Drain (LDD)
5. Source-Drain Implant/Diffusion
6. Salicide Formation/Contact Holes
7. Tungsten plugs + First Level Metallization
8. Additional Metal Layers
9. Passivation Layer and Bonding Pads

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### 1. N-Well Diffusion

Phosphorous Diffusion

(a)  $\text{SiO}_2$  /  $p$ -substrate

(b)  $n$ -well /  $p$ -substrate

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### 2. Active Area

Photoresist

(a)  $n$ -well /  $p$ -substrate

thick field oxide provides isolation between MOSFETs

(b) active region /  $\text{SiO}_2$  / active region /  $n$ -well /  $p$ -substrate

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### 3. Poly Gate

thin oxide (100–300Å)

(a)  $\text{SiO}_2$  /  $n$ -well /  $p$ -substrate

polysilicon gate

(b)  $\text{SiO}_2$  /  $n$ -well /  $p$ -substrate

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### 4. $n^+$ Source-Drain Diffusion

Arsenic Diffusion

(a)  $\text{SiO}_2$  /  $n$ -well /  $p$ -substrate

NMOS source /  $n^+$  / NMOS drain /  $n^+$  /  $\text{SiO}_2$  /  $n$ -well tap /  $n$ -well /  $p$ -substrate

(b)  $n^+$  /  $n^+$  /  $\text{SiO}_2$  /  $n$ -well /  $p$ -substrate

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### 5. p<sup>+</sup> Source-Drain Diffusion

(a) Boron Diffusion

(b) V<sub>DD</sub> tap, PMOS drain, PMOS source

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### 6. Contact Holes

(a) oxide layer over entire wafer

(b) etched contact holes

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### 7. First Level Metallization

(a)

(b) aluminium interconnect

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### Cross-Section and Top Down

Legend:

- METAL1
- POLY
- CONTACT
- N DIFFUSION
- P DIFFUSION
- N-WELL

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### More Process Steps

- Most devices require multiple levels of metallization
  - Deposit interlayer dielectric (ILD)
  - Pattern vias and trenches
  - Fill with copper

Source: IBM, 2005

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### Lecture 9: What have we learned?

- Be able to list the basic steps in the CMOS process flow
- Given a list of processes steps, put them in the correct order
- Be able to find the transistors when looking at a top-down design view

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