CHE323/CHE384
Chemical Processes for Micro- and Nanofabrication

Lecture 9
CMOS Process Flow

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Reading:
Chapter 16, Fabrication Engineering at the Micro- and Nanoscale, 4th edition, Campbell

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Basic CMOS Process Flow

0. Wafer Prep: Laser Scribe, Clean, gettering, 0th layer Alignment Marks
1. N-Well and P-Well Diffusion
2. Active Area
3. Polysilicon Gate
4. Lightly Doped Drain (LDD)
5. Source-Drain Implant/Diffusion
6. Salicide Formation/Contact Holes
7. Tungsten plugs + First Level Metallization
8. Additional Metal Layers
9. Passivation Layer and Bonding Pads

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1. N-Well Diffusion

2. Active Area

3. Poly Gate

4. n+ Source-Drain Diffusion
More Process Steps

- Most devices require multiple levels of metallization
  - Deposit interlayer dielectric (ILD)
  - Pattern vias and trenches
  - Fill with copper

Lecture 9: What have we learned?

- Be able to list the basic steps in the CMOS process flow
- Given a list of processes steps, put them in the correct order
- Be able to find the transistors when looking at a top-down design view

Source: IBM, 2005