Modeling and characterization of a 0.5 μm deep ultraviolet process

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A half-micron semiconductor manufacturing process using excimer laser lithography, single-layer chemically amplified resist on antireflective coating (ARC), and dry etch processes with *in situ* ARC development is discussed. Process window characterization experiments, long-term process stability/repeatability data, and initial defect test results are presented. Results show that the complexities added to the process by the incorporation of the ARC are outweighed by the improvement in linewidth control. Additionally, modeling of the lithography process is shown to accurately predict the process window and other lithographic effects.

I. INTRODUCTION

In order to meet the lithographic requirements for the production of sub-half micron devices, deep ultraviolet (DUV) exposure wavelengths are being investigated. In particular, step-and-repeat exposure tools using the 248 nm wavelength of the KrF excimer laser are considered a likely candidate for future semiconductor manufacturing. At DUV exposure wavelengths many technical problems are encountered. Some of the difficulties include complicated exposure tools, new resist chemistries and etching processes requirements, and the small processing windows which result when patterning half micron and smaller features. In addition, the increased substrate reflectivity usually encountered at the DUV wavelengths causes large variations in linewidth over topography. This paper discusses our approach to understanding and eliminating the barriers to a production worthy DUV process.

A new class of photoresist materials, called chemically amplified resists, are being developed to meet the needs of DUV lithography. Understanding the performance of these resists from theoretical and practical viewpoints is an important part of developing a manufacturable process. Modeling is an excellent tool for relating theoretical understanding to practical experience. The chemistry of chemically amplified resists can be modeled using the lithography simulation program PROLITH/2. This model has been used to investigate focus and exposure latitudes and the effect of antireflective coating (ARC) on the resist profile. Select results of this simulation effort, which demonstrate the ability of lithography modeling to accurately predict process windows, will be presented.

The small lithography processing windows associated with half micron and smaller features makes control of process errors critical. One error which is built into any single-layer resist process is the change in resist thickness over topography. If the substrate is reflective, the resultant linewidth will change over topography due to thin-film interference effects (sometimes called the swing-curve effect). One solution is to render the substrate nonreflective using an absorbing antireflective coating (ARC) under the photoresist. A good ARC material should reduce the reflectivity of the substrate to a few percent or less. Since this coating is below the photoresist, it must be patterned. Conventional wet etching of the ARC is not acceptable for fine patterning. Dry development of the ARC must be used because of the directionality of reactive ion etching (RIE) processing. The added process complexity of this etch can be alleviated if the etching can be performed *in situ*, i.e., directly preceding and in the same chamber as the substrate etch. The production worthiness of an *in situ* ARC etch process will be discussed in great detail.

Use of an ARC makes the photolithographic process virtually independent of the substrate type. This insensitivity to substrate type makes possible a simple exposure monitor for lithographic process control. Based on the resist characteristic curve, this exposure monitor can be used to control and /or monitor the required exposure dose without using send-ahead linewidth measurement wafers. Results from this monitor are presented, including short-term and long-term repeatability data.

As a measure of the production worthiness of the process, defect test structures were used to measure continuity, bridging, opens, shorts, contact resistance, linewidth, and overlay. These tests produced high yield, with the exception of contact resistance. Problems encountered at the contact level are discussed and short-term and long-term solutions are suggested.

II. LITHOGRAPHIC MODELING

The kinetics of the exposure and catalyzed amplification of chemically amplified photoresists have been described elsewhere,[1,2] but will be reviewed here for the case of SNR248 (Shipley Co., Newton, MA). This negative resist is composed of a poly(p-vinyl)phenol resin, a photoacid generator (PAG), and a melamine cross-linking agent.[3] As the name implies, the photoacid generator forms a strong acid, H^+, when exposed to DUV light. The kinetics of the reaction are thought to be standard first order:

$$\frac{\partial G}{\partial t} = -CGI, \tag{1}$$

where G is the concentration of PAG at time t (the initial PAG concentration is G_0), I is the exposure intensity, and C is the exposure rate constant. For constant intensity, the rate equation can be solved for G:

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$$G = G_0 e^{-CIt}. \quad (2)$$

The acid concentration H is given by

$$H = G_0 - G = G_0 (1 - e^{-CIt}). \quad (3)$$

Exposure of the resist with an aerial image $I(x)$ results in an acid latent image $H(x)$. A post-exposure bake (PEB) is then used to thermally activate the melamine crosslinking agent. Catalyzed by the acid, the melamine causes crosslinking of the resin. Since the acid is not consumed by the reaction, H remains constant. Using X as the concentration of melamine crosslinking sites, these sites are consumed (i.e., are reacted with the resin) according to first-order kinetics:

$$\frac{\partial X}{\partial t'} = -C'XH, \quad (4)$$

where C' is the rate constant of the crosslinking reaction and t' is the bake time. Assuming H is constant, Eq. (4) can be solved for the concentration of crosslinked sites M:

$$M = X_0 (1 - e^{-C'Ht'}). \quad (5)$$

(Note: Although H^+ is not consumed by the reaction, the value of H is not locally constant. Diffusion during the PEB causes local changes in the acid concentration, thus requiring the use of a reaction-diffusion system of equations.[4] The approximation that H is constant is a reasonably good one, however, and only contributes a small amount of error.)

It is useful here to normalize the concentrations to some initial values. This results in a normalized acid concentration h and a normalized crosslinked concentration m:

$$h = H/G_0$$

and

$$m = M/X_0. \quad (6)$$

Equation (5) becomes

$$m = 1 - e^{-\alpha h}, \quad (7)$$

where α is a lumped "amplification" constant[2] equal to $G_0 C't'$. The result of the PEB is an amplified latent image $m(x)$, corresponding to an exposed latent image $h(x)$, resulting from the aerial image $I(x)$. The resist is now developed into the final resist profile. The development rate R can be related to the degree of crosslinking by using the same kinetic model of development used for standard positive photoresists[5,6]:

$$R = R_{max} \frac{(a+1)(1-m)^n}{a + (1-m)^n} + R_{min}, \quad (8)$$

where

$$a = \frac{n+1}{n-1}(1 - m_{th})^n$$

and R_{max} is the maximum development rate, R_{min} is the minimum development rate, n is the dissolution selectivity parameter, and m_{th} is the threshold value of m.

For many resists this development rate expression can be simplified. Often the value of m_{th} is a large negative number. When this is the case, the development rate simplifies to

$$R = R_{max}(1-m)^n + R_{min}. \quad (9)$$

Thus, an initial aerial image $I(x,y,z)$ can be translated into a development rate differential $R(x,y,z)$. A suitable algorithm can then be used to predict the resulting photoresist profile.

The above kinetics for chemically amplified photoresists are found in the lithography simulation program PROLITH/2 (FINLE Technologies, Plano, TX). Using this modeling program, resist profiles were simulated and compared to experimental results (details of the experimental conditions are given in the following section). The results are shown in Fig. 1(a) with the simulation conditions given in Fig. 1(b). Input parameters for the model were either obtained from the literature[1] or measured for our process.[2] The model predicts an exposure latitude of $\pm 11\%$ for a linewidth change of $\pm 10\%$. The close agreement between model and experiment (see the following sections) indicates that modeling can be a useful tool for accurately predicting the processing window of a lithographic process.

III. EXPERIMENT

Bare silicon, polysilicon, nitride, oxide, tungsten, and aluminum wafers were coated with XP89-131 resist, a version of SNR248 (Shipley Co., Newton, MA), on top of ARC DUV-03 (Brewer Science, Rolla, MO). The wafers were spin coated on a Flexifab track (MTI, Parsippany, NJ). The imaging was done on an ALS 5:1 KrF excimer laser stepper (GCA, Andover, MA), equipped with a 0.35 NA lens. Following the track post-exposure bake (PEB), the wafers were immersion developed using Shipley's MF312 CD13.5 developer. Defect test structures were fabricated using three masking levels: gate (polysilicon), contact (oxide), and metal 1 (tungsten). Polysilicon, oxide, and aluminum (metal 2) wafers were etched using the 5000E, 8310, and 8330 plasma etchers (Applied Materials, Santa Clara, CA), respectively. Tungsten wafers with a hardmask (nitride) overcoat were etched sequentially in an Applied Materials 8310 for the nitride and a 4400 etcher (Lam Research, Fremont, CA) for the tungsten.[7] The wafers were resist stripped using a plasma, solvent, and acid strip system. Polysilicon wafers were further subjected to two diffusion cycles in order to activate the dopant. Polysilicon wafers were electrically probed on the EM-1 electrical linewidth measurement system (Prometrix, Santa Clara, CA) and the defect test structures were probed using a 4062C test system (Hewlett–Packard, Palo Alto, CA). The remaining wafers (for resolution and etch demonstration) were examined using scanning electron microscopy (SEMs). Resist thickness was measured with an SM200 thickness monitor (Prometrix, Santa Clara, CA).

IV. LITHOGRAPHIC RESULTS

Basic lithographic characterization of our 0.5 μm process has been performed using standard techniques. Some of this work has been reported earlier[8,9] and will be reviewed here along with current developments. The approach has been to use electrical linewidth measurement techniques in parallel with scanning electron microscope (SEM) measurements in order to determine and optimize the process window. Results of the stability of an exposure monitor for controlling dose to size will also be presented.

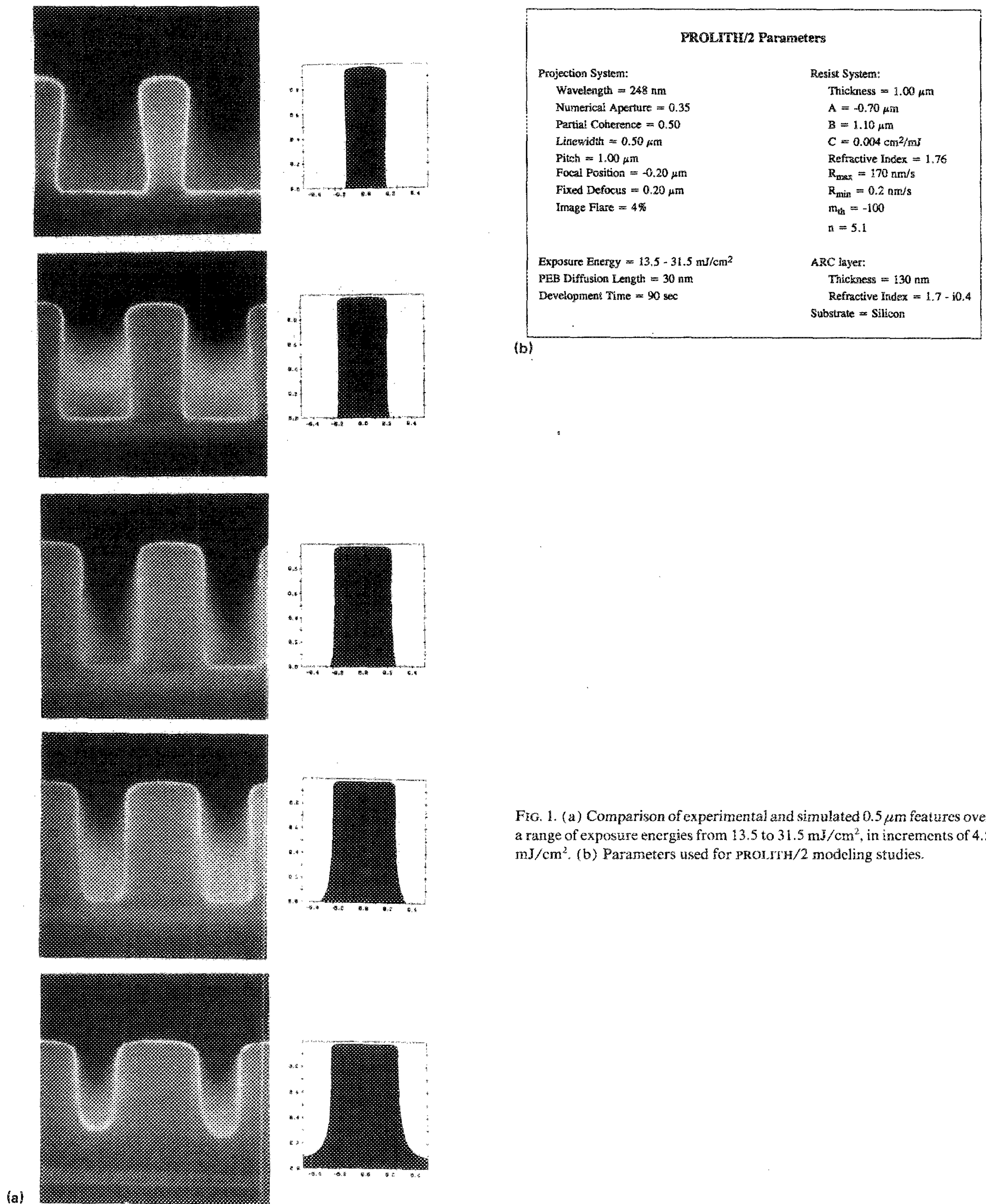


FIG. 1. (a) Comparison of experimental and simulated 0.5 μm features over a range of exposure energies from 13.5 to 31.5 mJ/cm^2, in increments of 4.5 mJ/cm^2. (b) Parameters used for PROLITH/2 modeling studies.

Sethi *et al.*[8] have reported the need for ARC to reduce substrate reflectivity in excimer laser DUV lithography as well as on an optimized lithography process. Figure 2 shows the improvement in the swing curve (the variation of linewidth with resist thickness) when an ARC is used on polysilicon. Using a design of experiments with focus and exposure latitudes as the responses, they showed the results of this optimized process (Table I). In this table, exposure

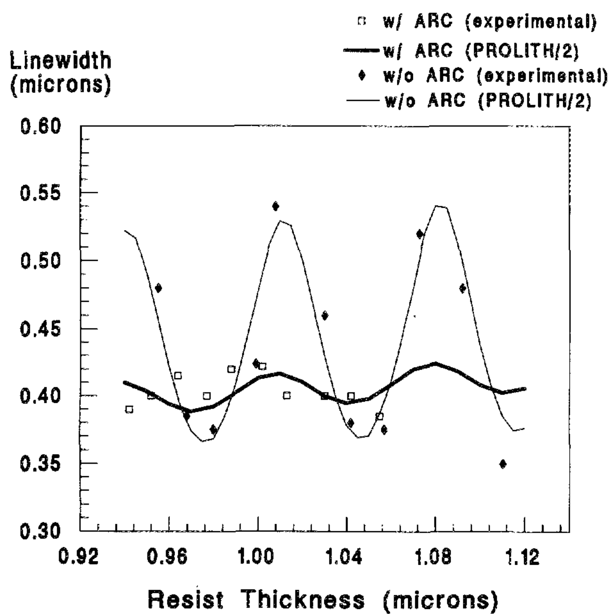


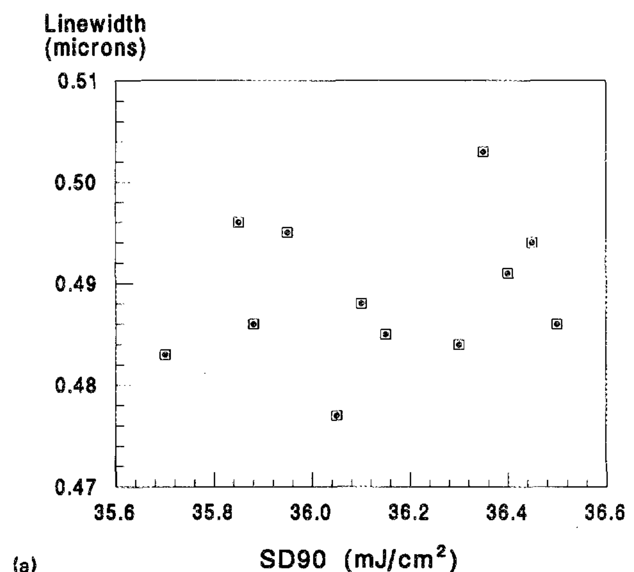
FIG. 2. CD variation as a function of resist thickness, with and without ARC (from Ref. 7).

latitude is defined as the maximum exposure dose variation that results in a critical dimension (CD) shift of less than ± 10% of the nominal linewidth over a focus range of 1.2 μm. Depth of focus (DOF) is defined as the total focus range which keeps the linewidth within ± 10% of the nominal over an exposure range of ± 10% of the nominal exposure. Experimental results showed that the exposure latitude was in excess of ± 10% when the depth of focus was ± 0.6 μm. The effect of the ARC is evident in the dose required for patterning nominal 0.5 μm geometries on polysilicon, nitride over tungsten, aluminum and nitride. The required dose is a function of the feature type being printed, but is insensitive to the substrate type.

Takemoto *et al.*[9] have reported on a technique to monitor the process stability for negative chemically amplified resists using the scumming dose at 90% resist thickness (SD90), based on the resist's characteristic curve. We have used this parameter to track the process with the purpose of eliminating send-ahead linewidth measurement wafers to determine dose to size. This parameter is insensitive to focus variations, and is thus used exclusively as an exposure monitor. Wafers were prepared as outlined in Ref. 9 and the SD90 parameters were extracted using an in-house software package according to the method of Takemoto.[9] Wafer linewidths were measured in a low-voltage in-line SEM. Figure 3(a) plots the critical dimension (CD) as a function of SD90 for all wafers within one lot (short-term correlation). The SD90 (hence dose to size) is very stable within one lot. Under these conditions, one SD90 measurement can be correlated to the linewidth within a lot to within ± 0.015 μm. The long-term correlation is shown in Fig. 3(b). (Note: the SD90 values are shifted between Figs. 3(a) and 3(b) because the experiments were performed on two steppers which were not dose calibrated to one another.) Using a correlation such as the one depicted in this figure, one can dial in the dose required to produce the nominal CD once the SD90 has been measured. This eliminates the need for send-ahead CD measurements.

TABLE I. Results of patterning 0.5 μm features on various substrates with ARC (from Ref. 7).

Substrate	Exp-Latitude	DOF	Dose
Poly-silicon	± 10%	± 0.6 μm	26 mJ/cm²
Nitride	± 10%	± 0.6 μm	26 mJ/cm²
Al-Si	± 11%	± 0.8 μm	26 mJ/cm²
Tungsten	± 11%	± 0.6 μm	27 mJ/cm²
Oxide (linear)	± 10%	± 0.6 μm	26 mJ/cm²
Oxide (contact)	± 10%	± 0.6 μm	20 mJ/cm²



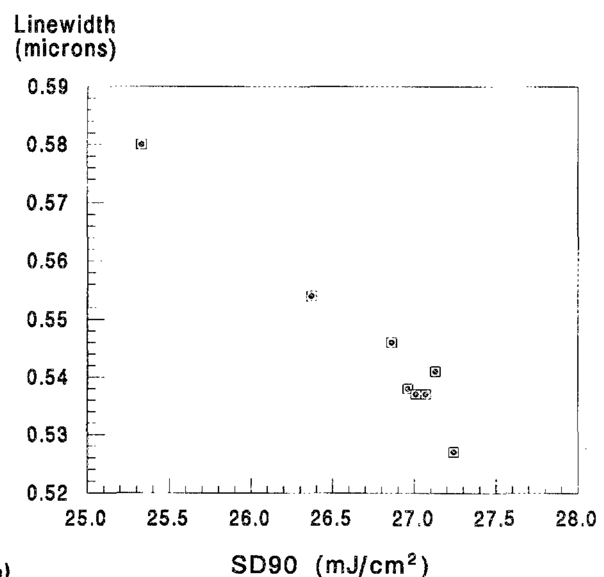


FIG. 3. (a) Short-term correlation of linewidth to the lithographic tracking parameter SD90. (b) Long-term correlation of linewidth to the lithographic tracking parameter SD90.

V. ETCH PROCESS DEVELOPMENT

As discussed previously, dry development of the antireflective coating is required for fine patterning. For process simplicity, the most desirable method of removing the ARC is *in situ* before beginning the etch of the substrate material. The goal of the *in situ* ARC etch is to cleanly remove the ARC while preserving the original lithographic linewidth and profile defined in the photoresist.

The ARC, being an organic material, was removed using an oxygen plasma. In order to achieve better directionality, an RIE type etch was used. We also investigated the incorporation of a noble gas, such as helium or argon, to aid in directionality. Due to the chemical nature of this process, some resist loss (and thus CD loss) was expected. ARC etch processes have been developed *in situ* before substrate etch for all levels in the reactors previously described. These processes were developed using statistically designed experiments and utilize oxygen alone or in combination with argon or helium. Results of gate, contact, metal 1, and metal 2 samples etched using *in situ* ARC and substrate etch processes are shown in Fig. 4. While the *in situ* processes have been successful on levels at contact and beyond, for isolation and gate mask levels a brief submersion in a buffered HF solution (1 min, 50:1 concentration) is required between the ARC and substrate etch processes. This additional step is needed to ensure a clean surface for the pattern transfer process.

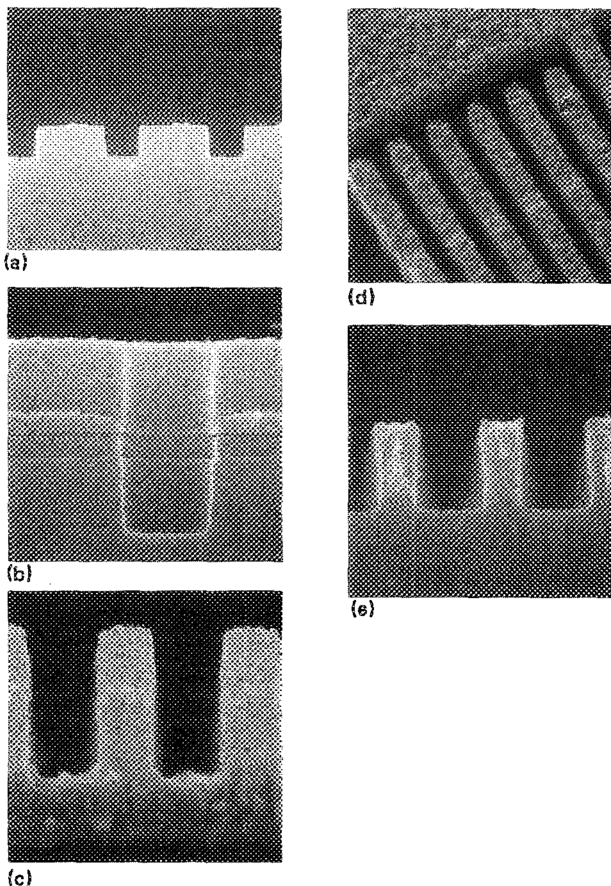


FIG. 4. Cross-sectional profiles for etched poly, contact, tungsten, and aluminum using *in situ* ARC and substrate etch processes: (a) 1.0 μm pitch poly, (b) 0.6 μm contact, (c) 1.0 μm pitch nitride hardmask on tungsten, (d) 1.0 μm pitch tungsten over topography, and (e) 1.0 μm pitch aluminum.

One of the major concerns about integrating a new material into a production line is the introduction of contaminants. Extensive analysis was carried out on the ARC material to assure that the integrity of the manufacturing process would be maintained. Table II shows trace metals analysis data for four standard *g*-line resist systems (resists A thru D).[10] Table II also contains ICP/MS data for the same trace metals on three different samples of the ARC material. While the earliest sample of ARC contained higher than desired levels of calcium and sodium (desired levels are well below 500 ppb), subsequent samples are well within the desired limits. The ARC samples also compare favorably with the commercial resist materials.

VI. OVERALL PROCESS STABILITY

A. CD Control

For the first linewidth stability test, polysilicon wafers were prepared using the ARC and XP89-131 resist process described above. Using full field Prometrix test patterns on two wafers, we electrically measured nominal 0.5 μm features at 72 sites per die, 37 die per wafer, for dense and isolated lines. The six sigma variation for all measurements was 0.08 μm. Moreover, the CD difference between dense and isolated features was only 0.01 μm. Note that these CDs are after etch and hence contain variations in both the lithography and etch processes. Correlations between electrical and SEM measurements of polysilicon lines have shown that the Prometrix consistently gives a result 0.1 μm less than the linewidth determined by the SEM. Further, the etch contributes a bias of approximately 0.1 μm relative to the photoresist linewidth. Thus, a 0.3 μm mean electrical CD corresponds to about a 0.5 μm mean photoresist linewidth. Figure 5 shows the distribution of CDs for all features in this test, with greater than 10 000 sites reported.

The second linewidth stability test investigated both the wafer-to-wafer and within-wafer variation of CD. Figure 6(a) shows the wafer-to-wafer variation of mean CD within one lot and Fig. 6(b) shows an example of the typical within-wafer variance demonstrated by this process. For these examples, the CD was approximately 0.65 μm before etch. The data represent the overall variance contributed by the lithography, etch and film properties (thickness and doping level), and typically shows a three sigma value of less than 0.1 μm. The error bars in Fig. 6(a) represent ± 1 standard deviation for the within-wafer measurements.

The ARC etch process used in this study yielded a very reproducible 0.1 μm etch bias. Subsequent experiments have shown that the CD loss can be reduced to near zero by adjusting the etch process parameters, specifically the ratio of oxygen to helium or argon, the cathode temperature and the presence of a fluorine containing gas. The results of this work will be presented at a later date.

TABLE II. Comparison of trace metals analysis (ppb) for ARC samples and commercial photoresists.

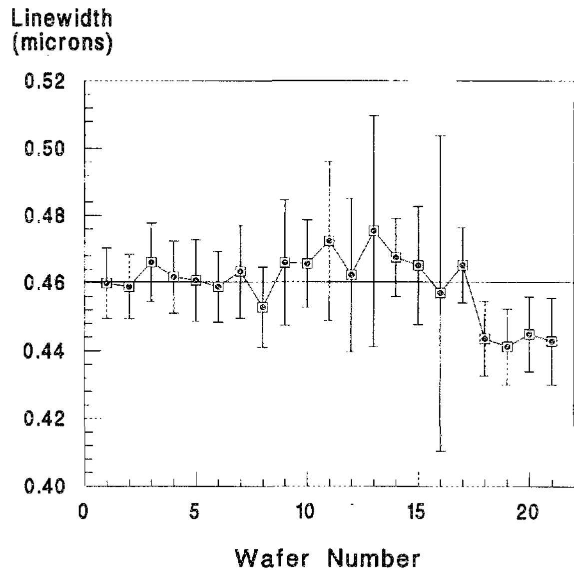
Trace metal	Resist A[a]	Resist B[a]	Resist C[a]	Resist D[a]	ARC 1	ARC 2	ARC 3
Al	4.6	6.7	11	3.4	1.7	1.7	2.4
Ca	100	34	34	6.4	380	4.5	*N/A*
Cr	72	92	130	36	5	2	1.4
Cu	41	34	40	14	5.3	1.7	*N/A*
Fe	280	100	93	23	22	22	18
Pb	2.2	3	2	2	0.9	0.3	0.6
Li	0.2	0.4	0.2	0.5	<0.1	<0.1	4.1
Mg	12	100	6.3	2.8	86	4.3	56
Mn	4.6	2.1	0.7	2	0.4	0.4	0.4
Ni	46	5.7	6.2	1.3	3.2	3.4	3
K	<5	24	15	9	30	<5	11
Na	200	250	350	7.7	680	1.6	17
Sn	6	6	6	3	1.1	0.7	*N/A*
Zn	10	63	4.3	3	15	3.3	18
Si	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	130

[a] From Ref. 10.

B. Effect of *in situ* ARC etch process on the etching chamber

The system used to perform polysilicon etch in this study was an Applied Materials 5000E. The polysilicon etch process itself was similar to the manufacturer's recommended process, utilizing a Cl_2/HBr chemistry for the main etch, with the addition of a small amount of oxygen to the overetch to improve the selectivity of polysilicon to SiO_2. The ARC etch process utilizes oxygen and helium in the same reaction chamber as the substrate etching. Since most etching processes used at SEMATECH use an oxygen plasma or contain oxygen as one of the constituent gases, the stability of this reactor can be used as a gauge for evaluating the effect of the ARC material and the ARC etch process on overall reactor performance.

With the limited data available to date, no adverse effects of the ARC etching process on the subsequent substrate etch



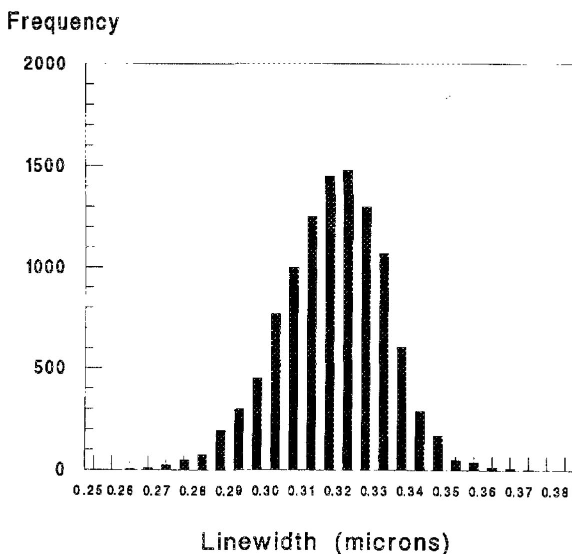


FIG. 5. Linewidth histogram for dense and isolated structures for a typical poly test lot (10 600 samples, mean = 0.318 μm, standard deviation = 0.016 μm).

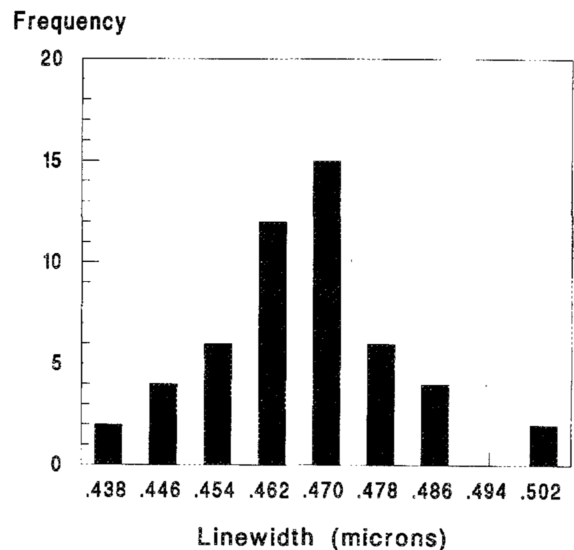


FIG. 6. (a) Wafer-to-wafer CD control within one lot (mean = 0.460 μm). Error bars show ±1 standard deviation for the measured within-wafer CD. (b) Within-wafer CD control for a typical poly test lot (mean = 0.466 μm, standard deviation = 0.012 μm).

process have been observed. Figure 7 shows a control chart for the polysilicon etch rate for this reactor. Since the reactor is also used to etch polysilicon lots which do not use ARC, arrows on the chart (designated "A") indicate when ARC etch processes were run. It can be seen that the ARC etch had no adverse effect on the etching rate or its standard deviation for these samples. In addition, cross-sectional SEMs taken during this time frame showed no polysilicon profile deviations induced by the ARC etch process.

VII. DEFECT TEST RESULTS

The vehicle used for defect yield testing was a three-level, 0.5 μm defect reticle set which allows electrical measurement of parameters such as continuity, bridging, opens, shorts, linewidth, overlay, and contact resistance. Both large-area and small-area structures were tested.

Two passes of the gate, contact and metal 1 defect test devices have been run and have shown good preliminary results. On the large and small area modules, yields of greater than 90% for x, y, and corner continuity structures were seen. Yields of 70% for large and small bridging structures were also seen. The smaller yields for bridging structures were attributed to an insufficient strip process that has since been corrected. Another problem that became evident was very low contact chain yields. Using a negative resist for contacts is known to be difficult due to imaging effects[11] and the etch bias in the process compounds this problem. In order to obtain etched 0.5 μm contacts, the resist must be overexposed to give 0.4 μm images. The net result is a process with a very small process window for producing contacts which do not scum at the bottom. The scumming leads to closed contacts, resulting in a high contact resistance for the contact chain test. Currently, work is being done to eliminate the bias in etch, allowing the contacts to be properly imaged. A long-term solution to the problem of contact definition must include the development of a suitable positive DUV resist.

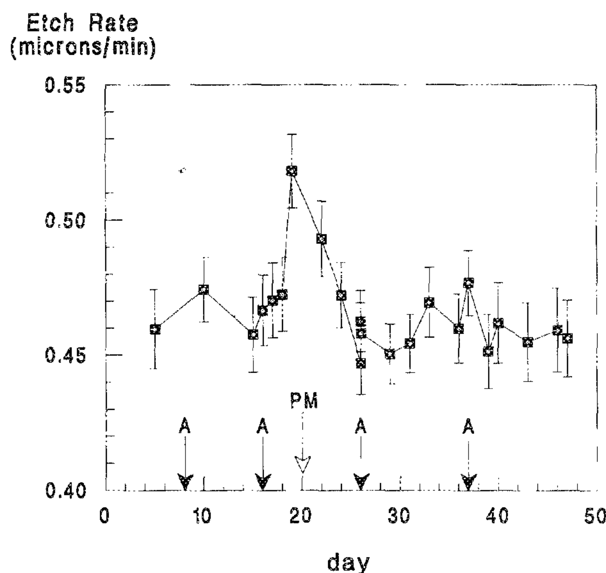


FIG. 7. Polysilicon etch rate including impact of ARC processing. *In situ* ARC etching was performed on days indicated by the symbol A, and preventative maintenance was performed as indicated by PM. Error bars show ± 1 standard deviation for the measured etch rate.

Optical verniers were used in an initial characterization of overlay performance and showed the overlay to be between 170 and 200 nm. Although this value is higher than desired, it was acceptable for initial work. It is expected that the next generation DUV stepper will have significantly better overlay capabilities.

Overall, the first two defect test passes showed good yields and gave valuable insight into problem areas. Currently, work is being done to eliminate any further yield detractors and to achieve yields of greater than 90% for all structures. Some corrective actions, such as a better strip process, have already been implemented. We are now beginning to run this test vehicle in volume to further evaluate the production worthiness of the DUV process.

VIII. CONCLUSIONS

The results presented here have shown that DUV lithography is manufacturable, but with some work yet to be done. Modeling of DUV lithography has predicted the process windows that were measured on actual wafers and was shown to be a valuable tool for process characterization and problem solving. With the integration of an organic ARC, the process became substrate insensitive and linewidth control was greatly improved. With SD90 implemented as an exposure monitor, the process no longer requires CD test wafers for determining dose to size. We have shown an overall final CD variation of less than 0.1 μm 6-sigma, and a process that images well over topography. Preliminary defect results are promising, however, the issue of imaging contacts with a negative resist/clear field reticle has yet to be adequately resolved. Characterizing problems by means of the defect test vehicle, we are addressing all issues in order for DUV to be a completely production worthy process.

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[b] On assignment from LSI Logic.
[c] On Assignment from Harris Coporation.

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