

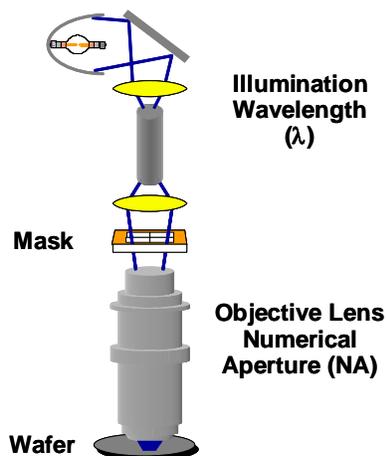
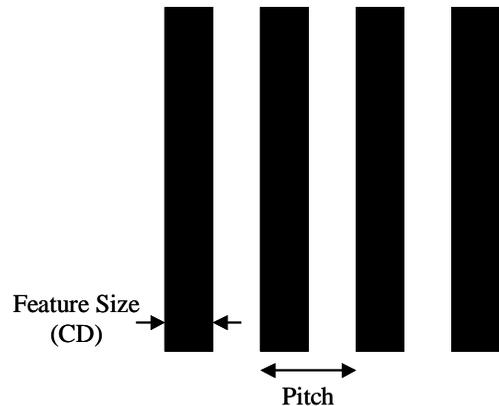
What's So Hard About Lithography?

Chris A. Mack, www.lithoguru.com, Austin, Texas

Optical lithography has been the mainstay of semiconductor patterning since the early days of integrated circuit production. The continual reduction of the dimensions of the features used to construct transistors has allowed these transistors to become ever smaller, faster, lower power-consuming, and cheaper. Historically, the smallest features on a wafer have been reduced in size by about 30% every two to three years. As a result, chips with features much less than 100nm across are in production today. Many technological barriers confront us when simultaneously shrinking transistor size and increasing the number of transistors on a chip. Ultimately, however, chip manufacturing has always been limited by our ability to print small features cost-effectively. As a result, the resolution limits of optical lithography tend to dictate the manufacturing capabilities of our industry. What limits our ability to print wafers with smaller dimensions? What are the implications of these limits to chip manufacturing?

Resolution

The resolution limit of optical lithography is not a simple function. In fact, resolution limits differ depending on what type of feature you are trying to print. In general, however, there are two types of resolution: the smallest pitch that you can print (the pitch resolution) and the smallest feature that you can print (the feature resolution). While related, these two resolutions are limited differently by the physics of lithography, and have different implications in terms of final device performance. Pitch resolution, the smallest linewidth + spacewidth pair that we can print, determines how closely we can pack transistors together on one chip. This resolution has the greatest impact on cost per function and functions per chip. Feature size resolution determines the characteristics and performance of an individual transistor, and has the greatest impact on chip speed and power consumption. Obviously both are very important.



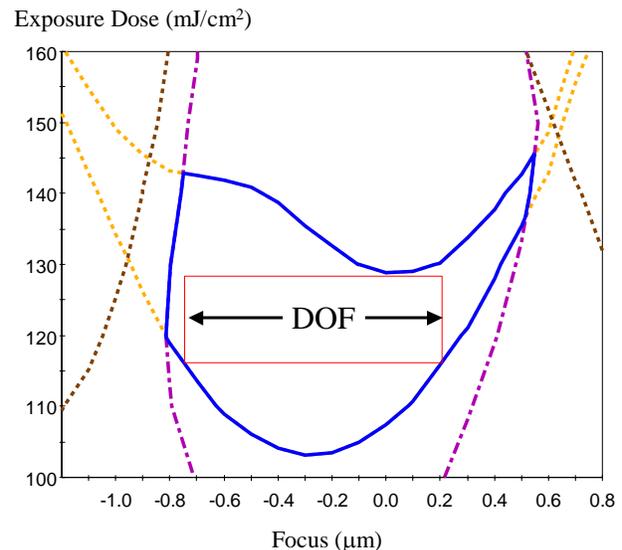
Pitch resolution is the classical resolution discussed in most optics textbooks and courses. It is governed by the wavelength of the light used to form the images and the numerical aperture of the imaging lens. The classical pitch resolution is given by a version of the Rayleigh equation

$$\text{pitch resolution} = k_{\text{pitch}} \frac{\lambda}{NA}$$

where λ is the vacuum wavelength of the lithographic imaging tool, NA is the numerical aperture, and k_{pitch} depends on the details of the imaging process [1]. Ultimately, k_{pitch} can be as low as 0.5, but only with tremendous effort (as will be discussed below). Values of 0.7 – 0.9 are more typical today.

While pitch resolution has a hard physical limit given by the Rayleigh equation, feature resolution is limited by our ability to control the critical dimension (CD) of the feature. As features are made smaller, our control of the CD of that feature is worse. There is no hard cut-off, only a worsening of CD control as the feature size is reduced. Feature size control is governed by the magnitude of various process errors that inevitably occur in a manufacturing environment (such as focus and exposure errors), and the response of the process to those errors. In order to improve CD control one must simultaneously reduce the sources of process errors and improve process latitude (the response of CD to an error). Interestingly, process latitude is similar to pitch resolution in that it also depends most strongly on the imaging wavelength and numerical aperture, though in more complicated ways.

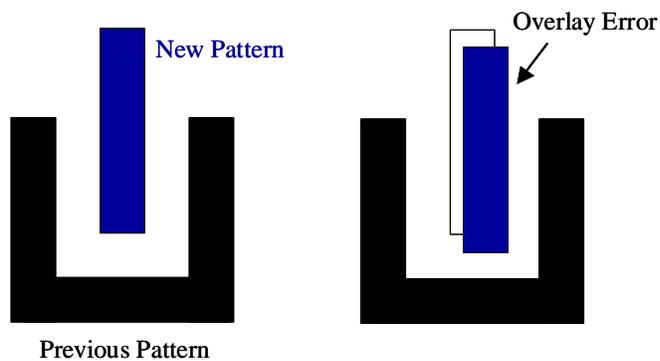
Process latitude is an exceedingly general concept, but usually the most important process latitudes are the interrelated responses of CD to focus and exposure. Using the process window to characterize these responses [2], we define depth of focus (DOF) as *the range of focus which keeps the resist profile of a given feature within all specifications (linewidth, but also sidewall angle and resist loss) over a specified exposure range* [3]. As any lithographer who has ever struggled with attempts to improve feature resolution knows, one of the most insidious problems of lithography is that small features tend to have smaller depth of focus. In fact, feature resolution can be succinctly defined as *the smallest feature of a given type which can be printed with a specified depth of focus* [4]. The specification for DOF is governed by the magnitude of the process errors present in the manufacturing process, while the DOF itself is used as a proxy for the full range of process latitudes that govern the resulting CD control.



Overlay – Lithography on Multiple Levels

The above description of resolution in semiconductor lithography ignores one important aspect of chip manufacturing – lithography is not done just once to make one chip, it is repeated many times. An integrated circuit is built up layer by layer to create a complex, three dimensional structure of many different materials. Anywhere from 20 to 30 separate lithography steps are performed on a wafer to create a modern chip. The limits of resolution, as discussed previously, apply to any one of these lithography steps. But there is another important type of resolution that relates to how one lithography step prints relative to a previous lithography step. When printing

a small pattern one must not only get the size of that feature correct, one must place that feature on the wafer at just the right spot so that it can work correctly with the patterns defined by previous lithography steps. Overlay is the measure of how well one pattern is placed on a wafer relative to a previously defined pattern.



Overlay errors have a definite impact on how small we can make the circuit device. Given a certain expected amount overlay error, the chip must be designed with enough room between the various components in order to tolerate these errors without causing device failure. As a result, the transistors are not as small and are not packed as tightly together as they might otherwise be. The biggest impact of adding tolerance for

overlay errors is a decrease in packing density and a subsequent increase in chip size. Like pitch resolution, overlay control affects price per function and functions per chip. Continuously improving our ability to control overlay is almost as important as improving our ability to control CD.

How can Resolution be Improved?

Since both pitch resolution and feature resolution are important, the following approaches are used to improve “resolution”:

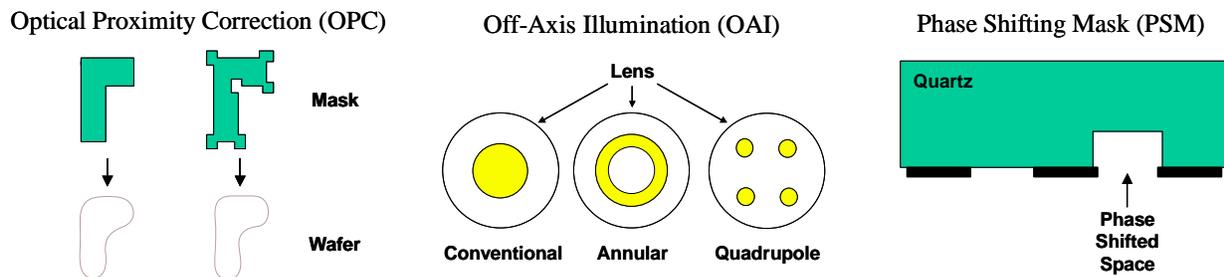
- Reduce the exposure wavelength
- Increase the imaging lens numerical aperture
- Reduce k_{pitch}
- Increase the focus-exposure process window size
- Reduce the magnitude of process errors such as focus and exposure errors

But here’s the rub: several of these factors work against each other. For a given feature, there is an optimum numerical aperture that gives the largest process window. Increasing the NA further will reduce the process window, making the feature resolution worse even as the pitch resolution is improved. Reducing wavelength is always good, but as a practical matter it is extraordinarily difficult since we are limited by our ability to engineer materials with the proper optical properties at the lower wavelength. Of course, reducing the magnitude of process errors is a never ending quest with cost being the only possible downside. That leaves two final resolution enhancement approaches: reducing k_{pitch} and increasing the size of the process window.

By far the most effective and popular process window improvement approach has been improvements in the photoresist. Over the years resist capabilities have undergone dramatic progress. While we are still far from being able to ignore the photoresist (meaning that resist properties in no way limit our lithographic capabilities), resist performance today is high enough that even small improvements in optical imaging can be seen in the final patterns.

Attempts to improve the process window by optical means (sometimes called optical “tricks”) include:

- Optimization of the mask pattern shape (called optical proximity correction, OPC)
- Optimization of the angles of light illuminating the mask (called off-axis illumination, OAI)
- Adding phase information to the mask in addition to intensity information (called phase shifting masks, PSM)
- Control of the polarization of the illumination (a technique too new to have an acronym yet)



Collectively, these optical approaches are known as resolution enhancement technologies (RETs) [5-7]. While some techniques improve feature resolution at the expense of pitch resolution, many of the RET approaches can improve pitch resolution and increase the process window simultaneously, a seemingly no-compromise path to resolution enhancement. However, the most promising RETs (especially the best PSM techniques) require a revolution in chip layout design that has yet to occur. Ultimately, a k_{pitch} as low as 0.5 is possible, but only for chips designed specifically to take advantage of these RETs.

Overlay, as a type of “resolution”, has historically been seen as independent of the other feature size resolutions. Lithographers were divided into CD engineers and overlay engineers, and there was not much need for them to interact. All of the many fine adjustments that the overlay engineers made to the stepper had no discernable impact on critical dimensions. Adjustments made by the CD engineer to the resist process or stepper dose and focus did not impact overlay enough to worry about. But as both CD and overlay requirements push down to the nanometer level we find that many of the same sources of CD errors are also causing overlay errors. Aberrations in the stepper or scanner cause not only CD errors but also pattern placement errors that vary across the field and are different for different pattern types. Even focus and exposure errors can affect overlay results and overlay measurements. And the use of non-perfect phase shift masks combine with all of the above errors in very complex ways to impact pattern placement. In the sub-100nm lithography world control of CD and control of overlay are beginning to merge.

What does the Future Hold?

So where does this leave the future of semiconductor lithography? Lithography is hard and getting harder. There will be no revolution that makes it easier again. The fundamental pitch limits require us to reduce wavelength (though a transition to 157nm has been abandoned and it is likely that 193nm will be the last mainstream wavelength), increase numerical aperture (immersion lithography are raising NAs above 1) and use strong RETs. Feature size resolution limits will take advantage of all of the pitch resolution enhancements, plus use improving photoresists and continuous process control improvements to push individual features to incredibly small sizes. Overlay control requirements will put increasing demands on exposure tool mechanical precision, as well as highly corrected lens aberrations to limit image distortion. However, the full potential of optical lithography will be unlocked only when chip design processes are modified to conform to the constraints of lithography's physical limits (a topic that has been recently dubbed "design for manufacturing"). In the end, our industry will optimize the technical trade-offs of lithography for the lowest cost production of chips that customers want.

References

1. C. A. Mack, "Pitch: The Other Resolution," *Microlithography World* (Summer 1998), pp. 23-24.
2. C. A. Mack, "Depth of Focus," *Microlithography World* (Spring 1995), pp. 20-21.
3. C. A. Mack, "Depth of Focus, part 2," *Microlithography World* (Autumn 1995), pp. 23-24.
4. C. A. Mack, "Resolution," *Microlithography World* (Winter 1997), pp. 16-17.
5. C. A. Mack, "Resolution Enhancement Technologies," *Microlithography World* (May 2003).
6. C. A. Mack, "Off-Axis Illumination," *Microlithography World* (August 2003).
7. C. A. Mack, "Scattering Bars," *Microlithography World* (November 2003).