CHE323/CHE384
Chemical Processes for Micro- and Nanofabrication

Lecture 3
Semiconductor Economics

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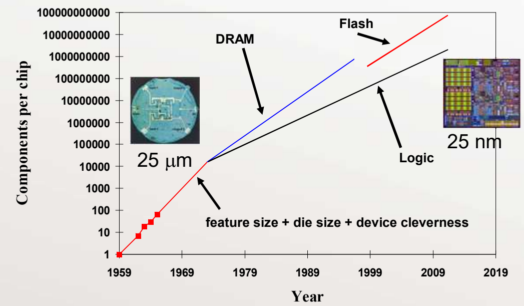
Reading:
Chapter 1, *Fabrication Engineering at the Micro- and Nanoscale*, 4th edition, Campbell

Moore's Law
"Doubling every 1 – 2 years"



Dennard's MOSFET Scaling Rules


Robert Dennard

Device/Circuit Parameter	Scaling Factor*
Device dimension/thickness	$1/\lambda$
Doping Concentration	λ
Voltage	$1/\lambda$
Current	$1/\lambda$
Capacitance	$1/\lambda$
Delay time	$1/\lambda$
Transistor power	$1/\lambda^2$
Power density	1

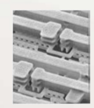
* Constant electric field scaling

There are no trade-offs. Everything gets better when you shrink a transistor!

IEEE Journal of Solid-State Circuits, Vol. SC-9, October 1974, pp. 256-268.

Dennard + Moore Today

- Dennard scaling is over - the only benefits of shrinking a transistor today are more functions/chip and/or lower cost/function
- Moore's Law cost: despite rising fab, equipment and material costs, and increasing process complexity, the cost/cm^2 of finished silicon has remained about constant over the years. How?
  - increasing yields
  - increasing equipment productivity
  - increasing wafer sizes



Chip Yield Trend

- 1970s
  - High volume yields of 20 – 40%
- 1980s
  - High volume yields of 40 – 60%
- 1990s
  - High volume yields of 70 – 90%
- 2000s
  - Trying hard to keep yields > 80% (and not always succeeding)

Lithography Costs
(single patterning)

	1979 g-line stepper	2004 ArF scanner	2012 ArF scanner
Wafer diameter (mm)	100	300	300
Tool throughput (wph)	18	100	240
Area throughput (cm^2/sec)	0.39	20	47
Tool cost (M$)	0.45	20	50
Tool cost (¢/cm^2)	0.65	0.65	0.67

(Note: this scaling requires that demand for chips increase by 100X)
(Assumes 5-year straight line depreciation, maintenance not included)

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Wafer Size Trend

- Time between wafer size increases is growing:

Year*	Wafer Diameter
1969	3 inch
1976	4 inch
1984	5,6 inch
1989	200mm
2000	300mm

Will 450mm wafers ever happen?

*first year of major production

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Wafer Size and Litho Costs

- Litho costs scale with area, not wafers
- Increasing wafer size means litho costs increase as a fraction of total costs

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Macroeconomic View

As with all commercial technology, economics has driven and will continue to drive the direction of IC manufacturing technology.

"…further miniaturization is less likely to be limited by the laws of physics than by the laws of economics."

Robert N. Noyce, 1977

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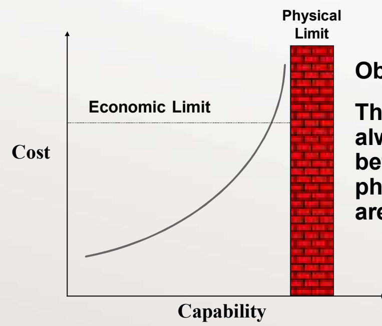
Technology vs. Economics



Observation:

The budget always runs out before the physical limits are reached.

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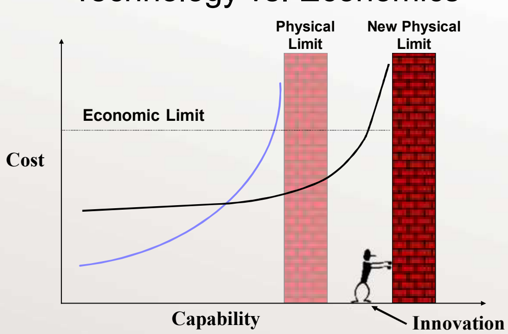
Technology vs. Economics



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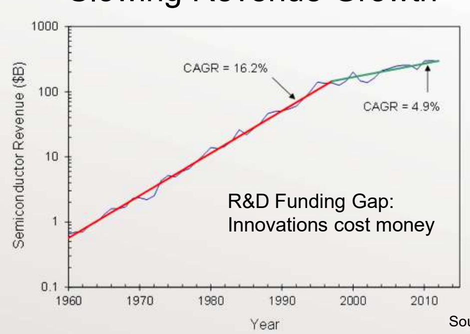
Slowing Revenue Growth



Source: SIA

Impact of Economics

- Slower semiconductor revenue growth is an inevitable sign of maturation
  - – Chips are saturating electronics: chip growth now limited to electronics growth
  - – Electronics is starting to saturate the world economy: maybe soon electronics growth will be limited to world economic growth
- Less revenue growth means less opportunity to invest in R&D

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Lecture 3: What have we learned?

- What are the current Moore's Law doubling rates for logic and flash?
- What is the fundamental economic principle of Moore's Law?
- What are three ways manufacturers have been able to lower the cost per transistor?
- How do lithography costs scale with wafer size?
- Why is Moore's Law getting harder to keep going?

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Additional Reading

- G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics* Vol. 38, No. 8 (Apr. 19, 1965) pp. 114-117.
- G. E. Moore, "Progress in Digital Integrated Electronics," *IEDM Technical Digest* (Washington, D.C.: 1975) pp. 11-13.
- G. E. Moore, "Lithography and the Future of Moore's Law," *Optical/Laser Microlithography VIII, Proc.*, SPIE vol. 2440, pp. 2-17, 1995.
- Chris A. Mack, "Fifty Years of Moore's Law", *IEEE Transactions On Semiconductor Manufacturing*, Vol. 24, No. 2 (May, 2011) pp. 202-207.
- Chris A. Mack, "The Multiple Lives of Moore's Law", *IEEE Spectrum*, pp. 30-37 (Apr. 2015).

