CHE323/CHE384
Chemical Processes for Micro- and Nanofabrication
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Lecture 55
Lithography: Linewidth Control

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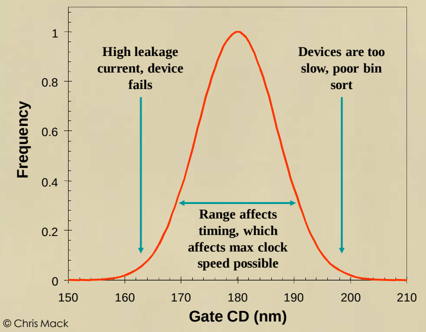
Linewidth Control

- Why is linewidth (or critical dimension, CD) control important?
  - The answer depends on the process layer
  - For all layers, CD control couples with overlay capability to determine the maximum packing density (i.e., design rules)
- Classic Example: gate CD control
  - Physical Result: gate switching time is proportional to gate length (for standard CMOS logic)
  - How does gate across chip linewidth variation (ACLV) affect device performance?

Poly Gate CD Control



- Smallest transistor limits reliability due to leakage current
- Largest transistor in critical path limits speed
- Range of transistors limits clock speed due to timing variation (skew)

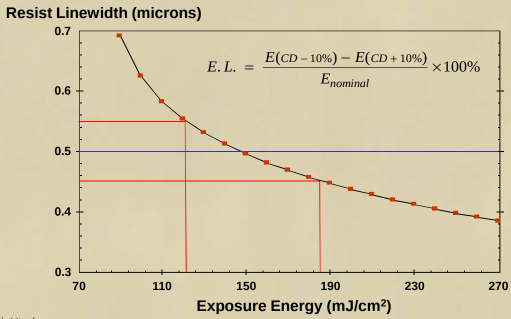
Linewidth Control Factors

- For small, uncoupled errors, CD variation can be expressed as

$$\Delta CD = \frac{\partial CD}{\partial v}\Delta v$$

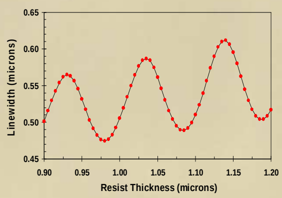
- Factors which determine linewidth control:
  - Magnitude of a process error (Δv)
  - Response of the process to that error, called the process latitude ($\partial CD/\partial v$)

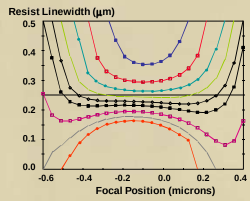
Exposure Latitude



Non-Linear Errors

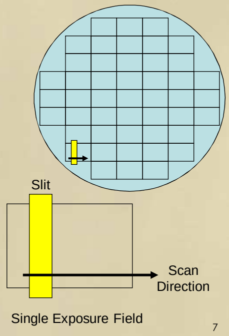
- Not all linewidth errors are linear!





Analyzing CD Errors

- Temporal Variations
  - Trend charts, SPC analysis
- Spatial Variations
  - Wafer-to-wafer, lot-to-lot
  - Across wafer
  - Across field
    - Slit direction
    - Scan direction
- Random Variations
- Two types of analysis
  - Sources of variations (bottoms up)
  - Statistical analysis of data (top down)



Analyzing Spatial Signatures

- Measure N wafers at many spatial (x,y) locations

$$M_i(x,y) = CD_0 + S_i(x,y) + R_i(x,y)$$

Measurement result from wafer *i*

Target CD

Systematic Error

Random Error

Analyzing Spatial Signatures

- Average over the N wafers at each (x,y) location to create a “composite wafer”

$$CCDE(x,y) = \frac{1}{N}\sum_i M_i(x,y) - CD_0 \approx S(x,y) + \frac{1}{N}\sum_i R_i(x,y)$$

Composite Wafer CD Error at each location

Systematic wafer signature

Random Error will average out to zero

Analyzing Spatial Signatures

- By determining the standard deviation of the residual for each wafer (the random errors), an estimate of the uncertainty in the systematic spatial signature can be made

$S(x,y) \approx CCDE(x,y)$ with an uncertainty of $\sigma_R(x,y)/\sqrt{N}$

- Similar analysis can give a composite field and composite slit

Linewidth Control Review

- Linewidth control is governed by two factors: the magnitude of a process error and the response of the process to that error
- Not all process errors are linear (e.g., swing curves, focus) nor independent (e.g., focus and dose)
- CD control has concrete impacts on device performance and yield
- CD errors are best characterized using bottom up (sources of variations) and top down (statistical spatial signatures) analysis

Lecture 55: What have we Learned?

- How does transistor gate CD variation affect the device?
- What two generic factors determine the resulting variation in CD?
- Name two process variables that result in quadratic rather than linear CD response
- Explain the difference between bottom-up and top-down CD error analysis

